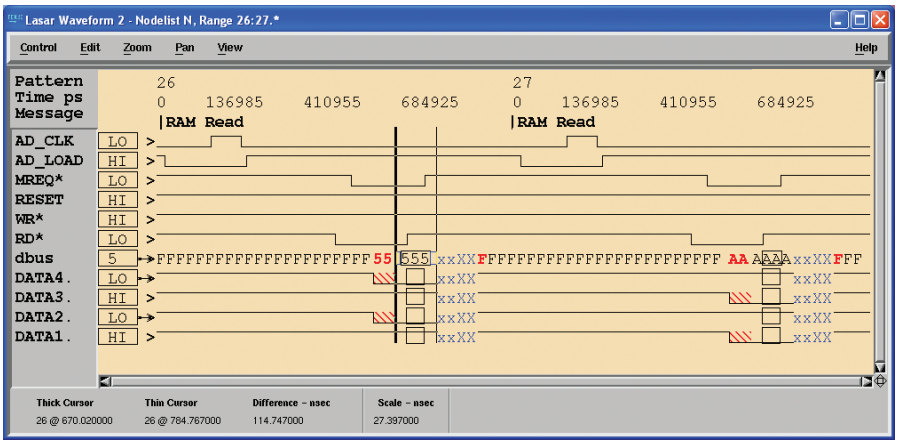
LASAR V6.60 Simulation System

The Defense Industry Standard for Digital TPS Development

Features

- Used by more than 3,000 TPS developers on more than 140 defense programs worldwide
- Menu-guided programming streamlines TPS development and brings new users up to speed fast
- SmartModel interface provides access to more than 11,000 simulation models available in the Synopsys DesignWare libraries
- Accurate guided-probe and fault-dictionary diagnostics ensure efficient fault isolation and repair
- Dynamic min/ max timing analysis and realistic fault simulation reduce tester integration time.
- Direct output to DoD-approved test equipment, commercial ATE, Teradyne's Spectrum-9100 Test Systems and Teradyne's Di-Series and M9-Series Digital Test Instruments
- LASAR V6.60 is available for OVMS, VMS, and Sun Solaris for SPARC Processors



LASAR V6.60 Speeds Test Development with Extended Simulation Model Support

For every innovation in digital device design or board assembly, there's a new challenge for functional test-and for test program developers. Developing reliable test programs for modern digital assemblies requires high-performance simulation and diagnostic tools and device models.

Teradyne's LASAR V6.60 software is the defense industry standard for generating digital test programs and diagnostics for high-speed functional testers. It is used in more than 140 defense electronics and avionics programs worldwide and is routinely specified by the U.S. Department of Defense (DoD) as a contract requirement.

Using dynamic min/max timing analysis, advanced simulation, and fault simulation algorithms, LASAR produces accurate, reliable test results. Test programs run reliably, right from the start, passing good boards and failing bad boards. Because LASAR accurately predicts how a board will behave under test, test programs can be debugged thoroughly in software, eliminating debug time on the tester.

Powerful New "Virtual Test" Tools for TPS developers

Model development can account for up to 40% of the time it takes to deliver a LASAR-based test program for a modern printed circuit board containing complex ASIC, FPGA, memory and VLSI devices. With V6.60 model availability is expanded and the development of models is more automated, making LASAR a more powerful test development tool than ever before.

LASAR V6.60 supports three times as many commercially available software models and ten times as many hardware models as earlier releases. This new option simplifies and automates the Synopsys SmartModel interface.

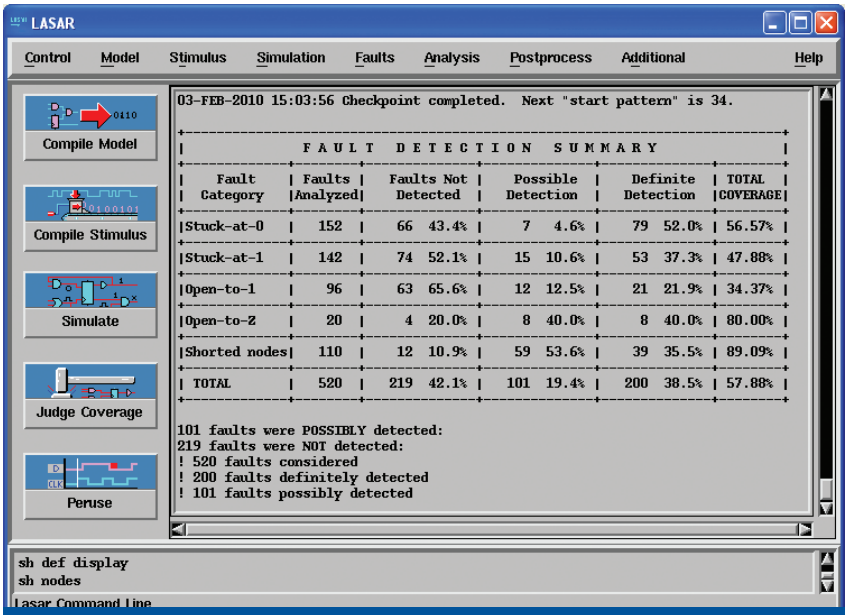
LASAR Interface to Synopsys SmartModel Libraries Leverages Development Investment

DesignWare SmartModels from Synopsys represent a large collection of commercially available, off the-shelf simulation models for memories, PALs, FPGAs, PLDs, SSI/ MSI, LSI and VLSI devices. These device models represent a reusable resource for TPS developers, which provides substantial leverage of the development investment.

With LASAR V6.60, TPS developers have access to Synopsys' extensive SmartModel library. The SmartModel Interface Option allows developers to tap more than 11,000 device models for use in LASAR simulations. Most full-functional SmartModels accessible with this option support the full set of

LASAR simulation capabilities, including true min-max timing analysis and fault simulation.

SmartModel library packages from Synopsys are available on Sun Solaris platforms. Users who run LASAR on VMS platforms can take advantage of SmartModel access with a UNIX platform running the SmartModel Interface Option networked to their VMS node.



LASAR's Fault Detection Summary and Fault Isolation Resolution Graph are widely accepted as proof of contract compliance.

Teradyne LASAR V6.60 Highlights

Fast test development:

• Ability to select different levels of simulation and fault analysis minimizes the amount of data processed at each development step

• Data analysis tools help improve fault coverage and fault isolation without additional simulation

• Efficient simulation algorithms and concurrent fault simulation minimize runtimes during pattern development to increase fault coverage

• "Hot" buttons provide one-step operation for compile, simulation, and fault simulation

Minimum tester integration time:

• Tester environment modeling accounts for effects of channel skew and fixture delay on test windows, test results, and fault coverage

• Tester rules checking ensures stimulus patterns are compatible with test system limits

• Automatic probe-window placement, based on tester constraints and pattern activity, eliminates days of manual analysis

Links to design:

• Accepts design netlists in industry standard EDIF format

• Imports design netlists from popular CAE systems, including Mentor Graphics' Design Architect

Comprehensive modeling tools:

• Library of 5,000 field-proven device models includes detailed manufacturers' timing specs

• SmartModel Interface Option provides access to more than 11,000 simulation models from Synopsys

• Interface software to LM1400 and Model Source 3000 systems enables these hardware modelers to support LASAR simulations for diagnostic test program development

• RAMGEN/ROMGEN software generates models for memory devices

• CircuitMaker software generates PLD models from JEDEC files and popular device libraries

High-quality, repeatable TPSs:

• Accurate simulation of board behavior under test ensures that TPSs run reliably and repeatably across multiple tester platforms

• Dynamic min/max timing analysis accounts for acceptable variations in testers and boards during simulation and fault simulation

• Automatic removal of common ambiguity delays in reconverging signals ensures realistic analysis of timing hazards

• Accurate simulation of stuck-at 0, 1, Z, and X faults, and hard-to-diagnose opens and shorts, provides highest fault coverage

Accurate tests and diagnostics:

• Comprehensive test-generation capabilities, including go/no-go tests, guided-probe diagnostics, and faultdictionary diagnostics

• Advanced fault-simulation algorithms achieve definite detection of faults that cause X (unknown) states

• Accurate resolution of faults that prevent initialization or whose effects vary with current drive strength, such as bus faults and adjacent pin faults

• Thorough analysis of fault-detection redundancy maximizes diagnostic resolution

Proof of contractual compliance:

• Exceeds MIL-STD-883C procedure 5012, which defines the DoD's minimum fault simulation requirements

• Produces direct output to CASS, IFTE, TETS, RTCASS, VDATS and other military testers

• Outputs simulation results in Digital Test Interchange Format (DTIF), IEEE 1445

• Generates diagnostic-resolution and fault-coverage reports that are widely accepted as proof of contractual compliance

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